Lagarto RISCV on Silicon (1st Edition)

(RED2018-102384-T)

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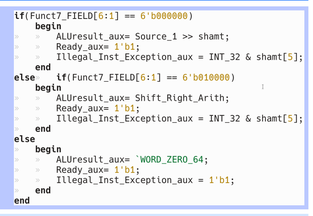
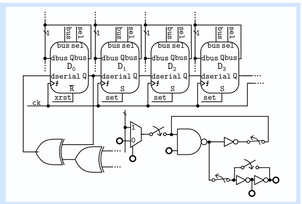
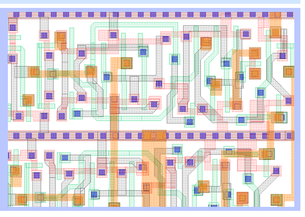
Lagarto is the first chip with RISC-V ISA open source developed in Spain and is an embryo of what the BSC intends the European processor to be

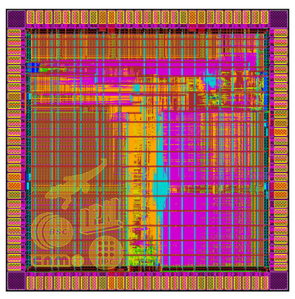
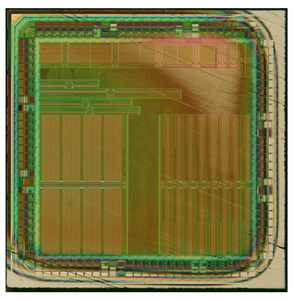
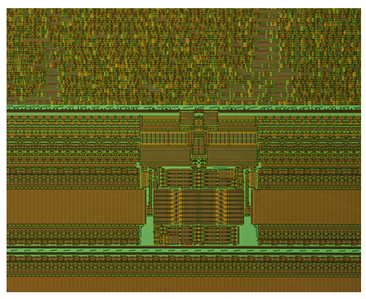
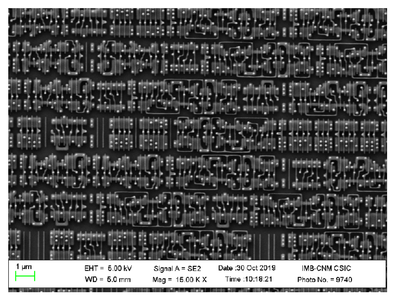
Lagarto Specifications

Concept	Initial Target FPGA	Target to fit in 2x2 mm^2
- Core processor: RISC-V 64IMA	- 5-stage, single-issue, in-order pipeline; bimodal branch predictor with 16K entries	- 5-stage, single-issue, in-order pipeline; bimodal branch predictor with 1K entries
- Caches: L1 instruction/data 4-way L2 shared 8-way	L1 32KB/32KB L2 256KB	- In-chip memories* L1 16KB/16KB L2 64KB *SRAM memories for register files and associated tables
- Peripherals	- JTAG; SPI controller; UART controller; DDR3 Memory controller	- JTAG; SPI controller; UART controller
- Memory Interface (IF)	- DDR3 Memory controller	- Custom FPGA-ASIC interface using only 68-bit bus
- Debug ring	- JTAG controlled; instruction-by-instruction execution; access to register/cache contents	- JTAG controlled; instruction-by-instruction execution; access to register/cache contents
- Target clock and area	- 200MHz clock; Xilinx Kintex KC705 FPGA	- 200MHZ clock; 2x2 mm^2 die area; <120 pins

Lagarto Implementation

Design Flow	Targets, Tools & Comments	Team [1]BSC, [2]IPN, [3]UPC, [4]CNM
Architectural Design 	Goals: Processor design Languages: Chisel, Verilog, SystemVerilog Tools: Xilinx Vivado, Mentor QuestaSIM Issues: Technology compliance	Jaume Abella[1], Guillem Cabo[1], Francisco Cazorla[1], Adrian Cristal[1], Roger Figueras[1], Alberto González[1], Carles Hernández[1], César Hernández[2], Vatistas Kostalampros[1], Neiel I. Leyva[2], Joan Marimon[1], Ricardo Martínez[4], Jonnatan Mendoza[1], Francesc Moll[3], Miquel Moretó[1], Julian Pavón[1], Cristóbal Ramírez[1], Marco A. Ramírez[2], Carlos Rojas[1], Antonio Rubio[3], Abraham Ruiz[1], Nehir Sonmez[1], Lluís Terés[4], Osman Unsal[1], Mateo Valero[1], Iván Vargas[1], Luís Villa[2]
RTL Synthesis Processes 	Goals: 200MHz clock frequency Tools: Cadence Genus Issues: Timing / corners Tech: TSMC-65nm through Europractice	
Physical Design Processes 	Goals: 2x2 mm^2 die area Tools: Cadence Innovus Issues: (main) area -> number of pins Tech: TSMC-65nm through Europractice	

Lagarto Results Summary

Concept	Results
- Fabricated chip (TSMC CMOS-65nm 1P6M)	- 2x2 mm^2 die area (0.57 mm^2 core processor); 108 pins
- RISC-V ISA tests	- All tests passed successfully
- Baremetal applications (bubble sort, Matrix Mul, Tower of Hanoi,...)	- Successfully executed
- Applications to create and modify a text file located in the SD Card	- SPI issue: successfully executed with equivalent functions on FPGA
- Linux Booting	- Successfully executed

The Most ...

... Important:
- The impressive team quality, commitment and motivation

... Challenging:
- Lagarto to Silicon in 5 months and running at first attempt

... Popular:
- Media coverage

... Exciting:
- Chip outboxing and first "Hello World..." from Lagarto chip
- Coming opportunities and challenges around RISC-V based OPEN Hw/Sw