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GAP: Grupo de Arquitecturas Paralelas

DISCA: Informática de Sistemas y Computadores

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Mission

Design better architectures, ranging from High Performance systems to embedded systems. Improve performance and energy efficiency of high-performance interconnects both for HPC and embedded systems.

Vision

Optimize system performance by an efficient co-design of all components, with special emphasis on the interconnect and its implications.

Group Profile

Research

- **NoCs & High Performance Interconnects**
  - Topologies
  - Routing algorithms
  - Congestion management
  - Etc. (any related aspect)
- **Architectures**
  - FPGA-based
  - Manycore architectures
  - Networks-on-chip
  - Coherence protocols

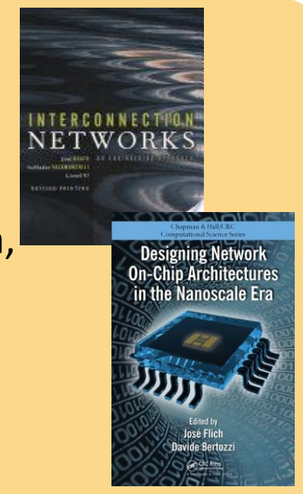
Recent / Ongoing Results

- **NaNoC (EU FP7)**: Nanoscale Silicon-Aware Network-on-Chip Design Platform
- **vIrtical (EU FP7):** SW/HW extensions for heterogenous multicore platforms
- **MANGO (FETHPC H2020):** exploring Manycore Architectures for Next-GeneratiOn HPC systems
- **RECIPE (FETHPC H2020):** Reliable power and time-ConstraInts-aware Predictive management on heterogeneous Exascale systems
- **DeepHealth (ICT, H2020):** Deep-Learning and HPC to Boost Biomedical Applications for Health
- **SELENE (ICT, H2020):** Self-monitored Dependable platform for Safety-Critical Systems
- **FRACTAL (ECSEL)**: A Cognitive Fractal and Secure EDGE based on an unique Open-Safe-Reliable-Low Power Hardware Platform Node

Training/Teaching

- **Computer Architecture (Degree)**
- **Advanced Architectures (Degree)**
  - Multicore architectures
  - High Performance Interconnects
- **Networks-on-Chip (Master)**
- **MIPS simulator** for teaching (in-order & out-of-order issue), being adapted to RISCV

- **Books:**
  - Interconnection Networks, an Engineering Approach, Morgan Kaufman
  - Designing Network On-Chip Architectures in the Nanoscale Era, CRC Press
- **PEAK manycore (MANGO):** Customizable manycore architecture based on MIPS ISA (being adapted to RISCV) with support for coherence protocols and Network-on-Chip



Innovation

- **BlueGene/L:** Fully Adaptive routing algorithm
- **DESTRO:** Efficient load-balanced routing for Multistage Interconnection Netwoks
- **RECN**: Dynamic Congestion Management strategy for Advanced Switching interconnect
- **LBDR**: Logic-Based Distributed Routing for NoCs

- **MANGO prototype:**
  - 96 high-end FPGAs interconnected in two racks
  - Pluggable I/O and DDR memories on top of FPGAs
  - Software runtime adapted to multi-FPGA setting

Group positioning & Perspectives in front of Open-Hw & RISC-V

R+D+i+T

- **Development of open-source simulators for RISC-V ISA**
- **Currently adapting PEAK manycore to RISC-V architectures, with provisioning for NoC and coherence protocols**
- **Development of accelerators for RISC-V architectures addressing Artificial Intelligence algorithms**
- **Use of RISC-V cores on current ongoing projects (SELENE, FRACTAL)**

Global Remarks

"To foster open source development and enrich academia and research groups with robust and powerful ISA. Enabling realistic processor designs with accepted ISA and in a growing ecosystem with accompanying tools and methods."

"Students will be highly motivated by the availability of real processors and the possibilities they will have to influence on processor designs and optimizations."