HIPICS: High Performance Integrated Circuits And Systems Design

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Mission

Design of integrated circuits which are robust in front of physical effects present in advanced technologies: signal and power integrity, device variability, device defects.

Vision

Improve the reliability and robustness of cutting edge and future technologies taking into account and linking device characteristics and circuit level solutions.

Group Profile

Research

- **RF CMOS design**
  - Aging, variability tolerance
- **Thermal testing**
- **Ultra low voltage digital design**
  - FDSOI technology, forward body bias
- **New computing paradigms**
  - New devices: memristors.
  - Fault tolerant, approximate computing, noise-driven computing
- **Energy Harvesting**

Training/Teaching

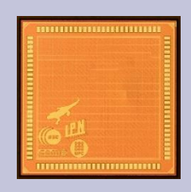
- **Digital Design**
- **Microelectronic Design**
- **Analog/RF IC Design**
- **IC Physical Design**
- **Energy Harvesting**

Tech Transfer

- **Design capability with experience in several technologies**
  - **AMS: 350nm**
  - **TSMC: 90nm, 65nm**
  - **UMC: 65nm**
  - **STMicroelectronics: 40nm, 28nm FDSOI**

Recent / Ongoing Activity

- **Maragda (TEC2013-45638-C3-2-R)** "Aproximación multinivel al diseño orientado a la fiabilidad de circuitos integrados analógicos y digitales"
- **Together (TEC2016-75151-C3-2-R) "**Towards Trusted Low-Power Things: Devices, Circuits and Architectures"
- **Lagarto-RISC-V (BSC-UPC-CNM):** 1st Spanish-Mexican RISC-V processor on TSMC-65nm silicon chip (via Europractice).



- **Bachelor (Grado) in Telecommunication Engineering (ETSETB UPC)**
- **Master in Telecommunication Engineering (ETSETB UPC)**
- **Master in Electronic Engineering (ETSETB UPC)**
- **(Professional) Master in IoT (UPCSchool)**
- **19 PhDs in the last 10 years**

- **Several projects with local companies (EPSON, Simon, Broadcom)**
  - UWB communications
  - Energy harvesting
- **Participation in 28 patents**
  - Thermal testing
  - Circuits

Group positioning & Perspectives in front of Open-Hw & RISC-V

R+D+i+T

- **Open Hw/Sw reduces dependency and facilitates collaborative projects and competitive markets.**
- **Open Hw as a common benchmark platform to apply research results.**
  - Ultra-low voltage.
  - Variability-aware/Approximate Computing.
  - On-chip RF communications.
- **Design of IP-Blocks for RISC-V.**
  - Body Bias Generators in FDSOI
  - On-chip Voltage Scaling blocks (DC-DC converters, configurable PLL...)
- **Use RISC-V as innovator driver-thread for universities and collaborative training strategies for all education levels.**

Further information on HIPICS group activity: https://futur.upc.edu/HIPICS