Computer Architecture and Parallel Systems

CAPS (UMU)

RED2018-102384-T

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Mission

High-performance and low energy consumption single- and multi-core architectures, covering design aspect in the processor, memory hierarchy, consistency model, ISA, and compiler.

Vision

Improve performance and reduce energy consumption thanks to the adequate support for speculation, hardware-software co-design, and efficient data movement in the memory hierarchy.

Group Profile

Research

- **Processor design**
- **Cache coherence protocols**
- **Memory hierarchy designs**
- **Memory consistency models**
  - RISC-V workshop
- **Hardware transactional memory**
  - Not defined in RISC-V
- **Software-Hardware co-design**
- **Simulation**

Recent / Ongoing Results

- **ECHO (ERC Consolidator Grant 819134)**: Extending Coherence for Hardware-Driven Optimizations in Multicore Architectures.
- **ECHO-Sync (ERC2018-092826)**: Efficient Synchronization in Multicore Architectures.
- **EPPEC (H2020 801051)**: European joint Effort toward a Highly Productive Programming Environment for Heterogeneous Exascale Computing.
- **MISSDI (RTI2018-098156-B-C53)**: Improvement of Infrastructures and Services ofr Innovative Distributed Systems.
- **Red-RISCV (RED2018-102384-T)**: Investigación, Formación e Innovación en Sistemas RISC-V.

Teaching

- **Computer architecture**
  - All courses (including Master)
- **Digital systems**
- **Operating systems**
- **Parallel programming**
  - CPU/GPU
- **TFGs on RISC-V**

- **Moving computer architecture teaching to RISC-V**
- **Extensions in the RARS simulator (for labs).**
  - New system calls.
  - Extend keyboard I/O functionality.
  - Run-time detection of calling convention violation.
- **Looking for suggestions for introducing RISC-V in computer architecture teaching**

Innovation

- **Patents**
- **Start Up**
  - Eta Scale AB

- **In contact with companies for transfer of technology.**
- **EuroLab-4-HPC (H2020-FETHPC-2014)**
- **Performed several evaluation projects with companies.**

Group positioning & Perspectives in front of Open-Hw & RISC-V

R+D+i

- **Introducing RISC-V as the main ISA for Computer Science Studies.**
- **Testing research ideas in real hardware.**
- **Improve performance of available RISC-V cores and looking for bottlenecks.**
- **Open Hardware is an important step to facilitate competitive markets.**

Global Remars

The new open RISC-V ISA opens an opportunity for easing building processors and systems on chip.

Our aim is first, to include RISC-V in the Computer Science degree, and then, port some of the research ideas to RISC-V systems looking for building commercial products resulting of our research.