# ArTeCS: Architecture and Technology of Computing Systems

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UCM

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## Mission

***Conception and construction of digital information processing systems, and its efficient application regarding performance, energy consumption, and cost paying special attention to HPC and processor & memory hierarchy design.***

## Vision

***Exploring the implications of specialization and heterogeneity at the architecture, system software and application level*** to face the new challenges and to exploit the new opportunities offered within the post-Moore era.

## Group Profile

### Research

- **Low Precision Arithmetic for DNNs (LNS, posits)**
- **Exploration of heterogeneous memory architectures**
- **Optimized BLAS ports to modern microarchitectures. Integration of DMA capabilities in BLAS libraries.**
- **Runtime and operating system scheduling. Hardware Performance Monitoring**
- **Code Generation and Optimization**

### Training/Teaching

- **Digital Design**
- **Computer Technology (FPGAs)**
- **Computer Organization and architecture**
- **Computer Science, Computer Engineering and Electronic Engineering degrees**
- **CS and IoT Master**

### Innovation

- **Embedded system design (e.g. IoT nodes)**
- **Low-level network optimizations**
- **Optimised libraries for heterogenous and/or special purpose architectures**
- **Performance monitoring tool PMCTrack: https://github.com/jcsaezal/pmctrack**

## Recent / Ongoing Results

- **SHARPE (PR65/19-22445)**: HW Support for The Acceleration of Expanded Scheduling via Reinforcement Learning
- **CABAHLA (CAM-P2018/TCS4423):** ConvergenciA Big dAtaHpc: de Los sensores a las Aplicaciones.
- **cHIMERA (RTI2018-093684-B-I00):** Heterogeneity and specialization In the post-Moore ERA.
- **Red-RISCV (RED2018-102384-T):** Investigación, Formación e Innovación en Sistemas RISC-V.
- **Development of RISC-Vfpga (Imagination Tech.)**

- **BSc and MSc Thesis related to RISC-V**
- **Posit+RocketChip: an Accelerator based on the Posit Number System**
- **Development of teaching materials for Introduction to Computers, Computer Organization and Computer Architecture based on the RISC-V architecture.**
- Analysis of the change of **Hardware** subjects on **RISC-V basis.**

- **Texas Instruments: "High Performance Dense Linear Algebra on Multicore DSPs". Part of the MCSDK-HPC toolkit for C66x DSPs by TI.**
- **IMEC: “Software controlled hybrid memory architecture exploration”. “Infrastructure for IoT memory organization”.**
- **Satlink: “Adaptation of the SOL Framework for the use of IoT oriented low Earth orbit satellite communications”.**
- **Indra: “Optimized FTP server & TCP/IP stack for TIP SRI“.**

## Group positioning & Perspectives in front of Open-Hw & RISC-V

### R+D+i+T

- **Open Hw/Sw RISC-V for accelerating time-consuming applications based on non-native formats (e.g. posits)**
- **Hardware Performance Monitoring on RISC-V**
- **Full port of dense linear algebra libraries (BLAS) to RISC-V (adaptation of the BLIS library).**
- **Design MLIR/LLVM Dialects to support RISC-V accelerator extensions.**
- **Use RISC-V as innovator driver-thread for universities and collaborative training strategies for all education levels.**
- **Just starting: “Implementación de un SoC RISC-V custom para IoT industrial”**

### Global Remarks

*“RISC-V architecture is a great opportunity to apply the lessons learnt in the past to the design of the new architectures for heterogeneous systems that can solve the challenges our society must face, taking into account security and energy (among others) as first order constraints.”*

*“The complexity of the challenges we are facing will require the joint work of scientists from different fields together with computer scientists, developing applications and middleware, in close cooperation with computer architects and technologists.”*