Computer Architecture and Technology

University of Cantabria (ATC-UC)

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Group overview

Arquitectura y Tecnología de Computadores (ATC) is a research group at the University of Cantabria. Its research focuses on the design, evaluation and application of today's computers, as well as those to come. Ensuring that computers carry out the tasks in a given program requires an adequate management of the billions of transistors that can be integrated in a chip. This complexity escalates in large computing systems where thousands of chips are interconnected.

Group Profile

Research

- **Memory and interconnection architectures**
  - Systems-on-Chip (SoCs), servers, datacenters and supercomputers.
- **Graph theory**
  - Application to interconnection networks and other data transmission problems
- **Architectural support for task oriented programming models.**
- Design and application of **general purpose GPUs and other acceleration devices.**

Training/Teaching

- **Computer Science** and **Telecommunications** engineering **degrees**
- **Computer Science** engineering **Master**
- Multiple classes related to:
  - **Computer organization & architecture**
  - Networking, Parallel programming
  - Operating systems & Datacenter

Innovation

- **Collaboration with multiple institutions:**
  - **BSC, UPC, U. Zaragoza**
  - **U. Adelaide, Australia; Trinity College, U. Dublín; Centro de Investigación en Computación, Instituto Politécnico Nacional, México; HLRS Stuttgart; ARM Research Cambridge; IBM; Atos**

Recent / Ongoing Results

- **Redes de Interconexión y Sistemas Heterogéneos (TIN2016-76635-C2-2-R)** Ministerio de Economía y Competitividad; Agencia Estatal de Investigación; Convocatoria Retos de la Sociedad (2016)
- **MONT BLANC 3: European Scalable and Power Efficient HPC Platform Based on Low-Power Embedded Technology** European Comission; H2020 (2015)
- **Red-RISCV (RED2018-102384-T):** Investigación, Formación e Innovación en Sistemas RISC-V.
- **Lagarto-Multicore (Collaboration):** Collaboration with BSC and IPN to build a multicore coherent system based on Lagarto & OpenPiton

- Designed and deployed **a Lab based on Raspberry-Pi**
  - RISC-OS, supporting both assembly & IO assignments
  - **!UCDebug** to support friendly debugging
- **Publication:**
  - "Tecnología low-cost para motivar al alumno", P. Fuentes, C. Camarero, C. Martínez, F. Vallejo. JENUI 2019
- **Exploring RISC-V alternatives for the lab.**

- **Relevant designs:**
  - Collaboration in the **merging of Lagarto & OpenPiton** to design a RISC-V cache-coherent multicore processor
  - **BST framework for design & synthesis of NOC routers with single- and multi-hop bypass.**
    - **Based on Booksim & OpenSMART**
    - **Required for high-performance multi-core designs**

R+D+i+T

- **Open HW/SW reduces dependency and facilitates collaborative projects and competitive markets.**
- **Open HW will reduce foreign technological dependence, becoming an strategic asset.**
- **Design of interconnects (NOC routers, memory coherence) and accelerators for RISC-V systems.**
- **Use of open hardware for undergraduate-level laboratories on computer architecture.**

Global Remarks

*"To consolidate the open hardware/software strategies based on the new RISC-V architectures, the synergies of the **prodigious circle "Research-Training-Innovation"** are required as an engine for a collaborative and joint evolution of the entire ecosystem that guarantees sustained, sustainable, cooperative and open progress "*

"The new open ISA RISC-V architectures offer an opportunity to improve technological independence, reduce oligopoly risks and facilitate market open competition"