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# Efficiently accelerating AI workloads with RISC-V



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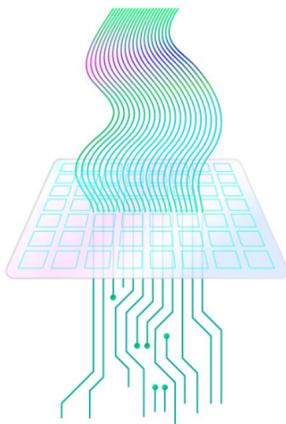
## Mission

For hardware and system designers who need the most energy-efficient, high-performance computing solutions for Artificial Intelligence and Machine Learning applications, Esperanto Technologies delivers solutions based on the open RISC-V instruction set architecture (ISA).

## Vision

Power consumption continues to be the most critical problem facing high-performance computing today. Our approach employs an array of over a thousand of our low-power ET-Minion cores, delivering energy efficiency with high integer and floating-point throughput, including tensor and vector acceleration optimized for ML / DL workloads.

## Breaking Barriers



Esperanto is creating a new generation of Artificial Intelligence (AI) / Machine Learning (ML) / Deep Learning (DL) processing solutions delivering unmatched energy efficiency (performance/watt), scalability, and flexibility. The historical limitations on many-core designs have always been complexity and power consumption, but it is now possible to create designs with over a thousand processor cores on one piece of silicon.

## Scalable



The Esperanto architecture is both regular and hierarchical, scalable in a number of dimensions to address different applications, different levels of performance, different power profiles and system form factors. This flexibility delivers optimal energy efficiency for each target application, be it at the edge or within the data center, with a family of architecturally consistent products. With over a thousand high-performance, energy-efficient 64-bit RISC-V cores on one chip, Esperanto can deliver TeraFlops of scalable compute performance.

## Energy Efficiency



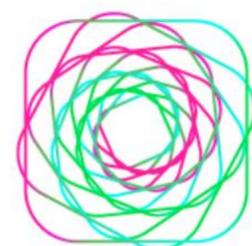
Delivering unmatched energy efficiency with unprecedented performance per watt.

## High Performance



Featuring the ultimate in performance, with architectures based on advanced ET-Maxion™ and ET-Minion™ cores.

## Innovation



Encouraging your innovation in artificial intelligence via flexible RISC-V open instruction set architecture (ISA) designs.