ICAS: Integrated Circuits And Systems

IMB-CNM (CSIC)

RED2018-102384-T

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Mission

Research and training on ***Micro/Nano-Electronic Devices, Circuits and Systems Design, Test and Deploy*** by means of SoA/new technologies, techniques and open architectures to improve the performances of multi-technology integrated solutions.

Vision

Improve, connect & exploit **the new "micro/nano-devices"** from different technologies within the "macro" framework of target end applications through smart interfaces developed including the appropriate degree of intelligence and moving to ***open hardware*** strategies and solutions.

Group Profile

Research

- **Low-Power Analog, Mixed & RF CMOS**
  - IR/XRay Imagers
  - Smart sensor frontends
  - IP blocks (DAC/ADC, PLL, …)
  - Open hardware and RISC-V based dev.
- **Printed/Organic-µelectronics**
  - Inkjet Printed Technologies & Devices
  - Organic Thin Film Transistors and Sensors
  - Printed Flexible Circuits

Training/Teaching

- **Digital Design**
- **Microelectronic Design & Test**
- Introduction to **Computer architecture**
- **Informatics, Telecomunication & Electronics** engineering degrees
- **Micro/Nano-Electronics Engineering Master**

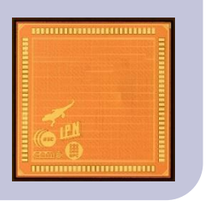
Innovation

- **In the past lots of industry-based R&D**
- **Now better balanced "research&Industry"**
- **IR/XRay-ROICs for imagers**
- **IP-blocks/chips for SilTerra, Arquimea/ESA, NIT.**
- **More technology transfer to SMEs on printed-organic µelectronics**

Recent / Ongoing Results

Research

- **LoHiRa ADC (ESA-NPI 553-2017)**: Low-Power High-Resolution Rad-Hard Analog-to-Digital Converters for Next-Generation Space Image Read-Out ICs
- **BrainCom (H2020-FETPROACT-Grant 732032):** Cortical implants as brain-computer interfaces for cognitive neuroscience applications.
- **EcoTronic (RTI2018-102070-B-C21):** Disposable Paper Electronic Devices for Sustainable Eco-friendly Platforms.
- **Red-RISCV (RED2018-102384-T):** Investigación, Formación e Innovación en Sistemas RISC-V.
- **Lagarto-RISC-V (BSC Contract):** 1st Spanish-Mexican RISC-V processor on TSMC-65nm silicon chip (via Europractice).

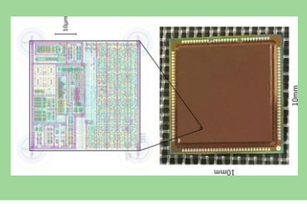


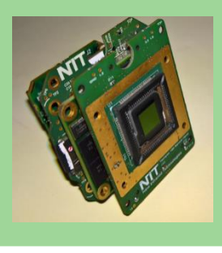
Training/Teaching

- **Mixed teaching courses: on-line (MOOC) & Classroom**
- **Publications:**
  - An Academic EDA Suite for the Full-Custom Design of Mixed-Mode Integrated Circuits, ISCAS-2017
  - Digital Systems: from Logic Gates to Processors. Springer, 2017.
  - Complex Digital Circuits. Springer 2019.
- **UAB** Engineering School: **Hardware** and **Computer Architecture** degree subjects **updated & harmonized** on a **RISC-V basis** (initial phase)

Innovation

- **Two IP-cores (Temperature sensor & Charge-pump) for SilTerra Co.**
- **Two ADC IP blocs designed for Arquimea/ESA consortium**
- **Three different IR-ROIC chip imagers (32x32, 80x80 and 128x128 pixels) transferred to NIT S.L.**





Group positioning & Perspectives in front of Open-Hw & RISC-V

R+D+i+T

- **Open Hw/Sw reduces dependency and facilitates collaborative projects and competitive markets.**
- **Freedom for evolution and helpful for training & education of new generations of professionals on Open Hw/Sw.**
- **IP-Blocks design (PLL, ADC, SerDes, Memory Ctrl., …) for RISC-V cores and related application developments.**
- **Low power RISC-V cores for IoT.**
- **Use RISC-V as innovator driver-thread for universities and collaborative training strategies for all education levels.**
- **Just starting an Industrial PhD around RISC-V core for IoT with NVision company**

Global Remarks

"To consolidate the open hardware/software strategies based on the new RISC-V architectures, the synergies of the ***prodigious circle "Research-Training-Innovation"*** *are required as an engine for a collaborative and joint evolution of the entire ecosystem that guarantees sustained, sustainable, cooperative and open progress "*

"The new open ISA RISC-V architectures offer an opportunity to improve technological independence, reduce oligopoly risks and facilitate market open competition"