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- **Título de la ponencia:**
  RISC-V and open hardware : opportunity and challenge for the EU

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- **Abstract:**
  While Moore's Law is not dead, it is slowing and becoming more difficult to sustain. New fabs are becoming cost prohibitive to build, stagnating the move to the next technology node and traditional CMOS scaling approaches have come to an end. In this new technology environment, some of the rules have changed. This has produced a shift from abundant transistors to efficient use of transistors. Thus, to truly meet the power and performance requirements, we must specialize the hardware. At the same time, the software stack is evolving, becoming more abstract, enabling higher programmer productivity, but sacrificing hardware efficiency. Thus, application owners will need to co-design the full stack, all layers of hardware and software, in order to meet their performance and power (FLOPs/W) targets. This level of integration is not possible in a closed or even partially open ecosystem. The platform must be open to enable this tight integration. We see this openness today in the Linux OS, toolchain, runtimes, frameworks, and libraries, up to the application layer. This enables rapid development and extension of software systems. However, an open hardware infrastructure is lacking, making specialization impossible. Openness is required to tailor your hardware platform to the applications, thereby achieving the desired performance in the power constrained environment.

  Mirroring the same model as Linux, RISC-V has followed a similar development path and has enjoyed significant industrial and academic adoption. Like Linux before it, the RISC-V ecosystem is in the nascent period where it can become the de facto open hardware platform of the future. The RISC-V ecosystem has the same opportunity in hardware that Linux created as a foundation for open source software. This enables the co-design of the RISC-V hardware and the entire software stack, creating a better overall solution than the closed hardware approach that is done today. As Europe HPC recognized in the past with Linux, Europe has the opportunity to lead the charge, creating a full stack solution for everything from supercomputers to IoT devices, all based on an open ISA, providing interoperability and a freedom to create, build, and deploy superior technology based on European IP. Barcelona Supercomputing Center (BSC) believes the future of the entire computing ecosystem will be based on open technology. Furthermore, to insure European participation and competitiveness in this technology race, Europe must embrace, support, and contribute to open source hardware in an enthusiastic manner, similar to its commitment to open source software. Barcelona Supercomputing Center (BSC) believes the future of the entire computing ecosystem will be based on open technology. Furthermore, to insure European participation and competitiveness in this technology race, Europe must embrace, support, and contribute to open source hardware in an enthusiastic manner, similar to its commitment to open source software. To demonstrate BSC's commitment, we are opening the Laboratory for Open Computer Architecture (LOCA), bringing all the pieces together, from applications all the way down to hardware. This is the critical missing piece that can kickstart the full stack open ecosystem, attracting Global industry, European talent, and government support. The focus of this center is to build high performance hardware for supercomputers to IoT, and everything in between. As an open training, research, and development

center, LOCA provides a global collaboration center for the sole purpose of developing leading edge hardware, in a co-design environment. MEEP is the first step for LOCA at BSC to build infrastructure to support software and hardware development. BSC provides the applications to drive the co-design process with the goal of targeting hardware pilots and other supercomputing projects to deploy hardware proofs of concept; the foundation for IP exploitation by industry and especially SMEs.

- **Biografía:**
  Mateo Valero, http://www.bsc.es/cv-mateo/. Director of the Barcelona Supercomputing Center. His research focuses on high performance architectures. Prof. Valero has been honoured with several awards, among them the 3 most relevant awards in Computer Architecture field : the Eckert-Mauchly Award 2007 by the IEEE and ACM; Seymour Cray Award 2015 by IEEE; Charles Babbage 2017 by IEEE; Harry Goode Award 2009 by IEEE:; the Spanish National awards "Julio Rey Pastor" and "Leonardo Torres Quevedo". "Hall of the Fame" member of the ICT European Program (selected as one of the 25 most influents European researchers in IT during the period 1983-2008. Lyon,November 2008); Honoured with "Condecoración de la Orden Mexicana del Águila Azteca" 2018, highest recognition granted by the Mexican Government. He is Honorary Doctorate by 9 Universities. He is member of 9 academies .He is a fellow of IEEE and ACM and he is also Intel Distinguished Research Fellow.