Red RISC-V:
Investigación, Formación e Innovación en Sistemas RISC-V

AGENCIA ESTATAL DE INVESTIGACIÓN
MICIU

1as Jornadas de la Red RISC-V

Barcelona, Campus UAB-Bellaterra, 5-6 de Febrero de 2020

- **Título de la ponencia:**
  Secure Foundational Exabyte HPC Systems for 2020 and Beyond SV/128-RISC-V

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- **Abstract:**
  In the last 40 years, for all practical purposes, the logical address space of various computers have doubled every 20 years or so. In 1978 DEC's VAX expanded from 16 to 32 bits. In the late 90's, SUN, HP, and INTEL expanded to 64 bits. In HP and INTEL's case, it was first ITANIUM, then for the IA-64 due to AMD's expansion from 32 to 64 bits. For all the above, the logical address expansion was architecturally defined, but not all the VA bits were interpreted. Meaning 48 of the 64 bits were interpreted. And recently INTEL expanded the interpretation of the IA-64 address space to 57 bits. In general, the availability of dense dram led to the need for expansion of the address space. Applications could always use the memory. In the technical world, data went from 1D to 2D to 3D, to finer meshes. In a more contemporary situation, the cluster wide addressing and web wide addressing (now via IPv6) has introduced new demands on data referencing. Additionally, while security concerns were always important, today they take on higher priority than previous thought. Micro-Architecture implementations that are used to increase performance, can result in security vulnerabilities. Yet all along we need to be upward compatible with existing instruction set architectures. SV128, specified for RISC-V attempts to meet these new requirements. SV128 is virtual address architecture NOT an ISA definition. There is NO attempt to define new user visible machine state. The 128 bit address space is partitioned into object_id and object offset. SV128 is also upward compatible with the RISC-V address spaces of RV32 and Rv64. Since SV128 is not an ISA definition, heterogeneous configuration of different ISA's can be configured sharing the same system-wide pointer format.

- **Biografía:**
  Wallach was a founder of Convey Computer. Micron Technologies acquired Convey in 2015. At Micron, Wallach is a design-engineering director. He retired from Micron on Aug 2019. Previously, he served as vice president of technology for Chiaro Networks Ltd., and as co-founder, chief technology officer and senior vice president of development of Convex Computer Corporation (NYSE). After Hewlett-Packard Co. bought Convex, Wallach became chief technology officer of HP's Enterprise Systems Group. Wallach served as a consultant to the U.S. Department of Energy's Advanced Simulation and Computing Program at Los Alamos National Laboratory from 1998 to 2007. He was also a visiting professor at Rice University in 1998 and 1999, and was manager of advanced development for Data General Corporation. His efforts on the MV/8000 are chronicled in Tracy Kidder's Pulitzer Prize winning book, "The Soul of a New Machine." Wallach, who has 40 American patents, is a member of the National Academy of Engineering, an IEEE Fellow, and was a founding member of the Presidential Information Technology Advisory Committee. He is the 2008 recipient of IEEE's Seymour Cray Award and the 2002 Charles Babbage award.